



PLL CIRCUIT AND OPTICAL COMMUNICATION RECEPTION APPARATUS

BACKGROUND OF THE INVENTION

This invention relates to a PLL (Phase Locked Loop) circuit and an optical communication reception apparatus, and more particularly to a PLL circuit which includes a phase detection circuit and a frequency detection circuit and an optical communication reception apparatus which uses a PLL circuit as a production circuit for a clock signal to be used for retiming processing of receive data.

FIG. 11 shows a configuration of a PLL circuit which is used commonly. Referring to FIG. 11, the PLL circuit shown includes a phase detection (PD) circuit 101 and a frequency detection (FD) circuit 102 and operates in the following manner.

First, the frequency detection circuit 102 performs phase comparison between an input signal DATA and clock signals (ICLK, QCLK). Then, the frequency of a frequency clock VCOCLK of a voltage-controlled oscillator (VCO) 106 is controlled through a charge pump (CP) circuit 104 and a loop filter 105 based on a result of the comparison to pull the oscillation frequency of the VCO 106 to a target oscillation frequency. The clock signals (ICLK, QCLK) are produced based on the oscillation frequency clock VCOCLK.

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